LH534600B

CMOS 4M (512K × 8/256K × 16)
Mask-Programmable ROM

FEATURES

- 524,288 words × 8 bit organization
  (Byte mode)
  262,144 words × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 100 ns (MAX.)
- Power consumption:
  Operating: 412.5 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
- ×16 word-wide pinout

DESCRIPTION

The LH534600B is a 4M-bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

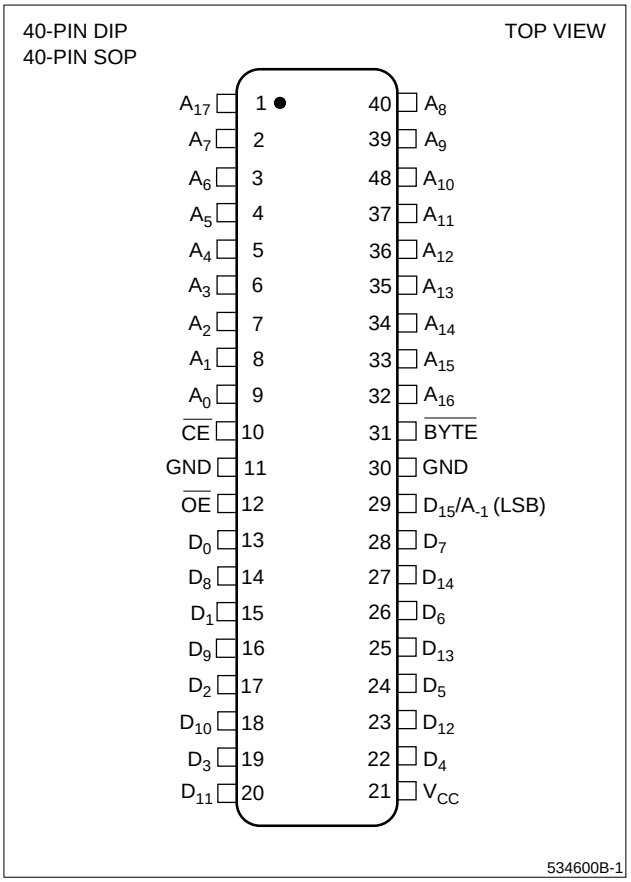


Figure 1. Pin Connections for DIP and SOP Packages

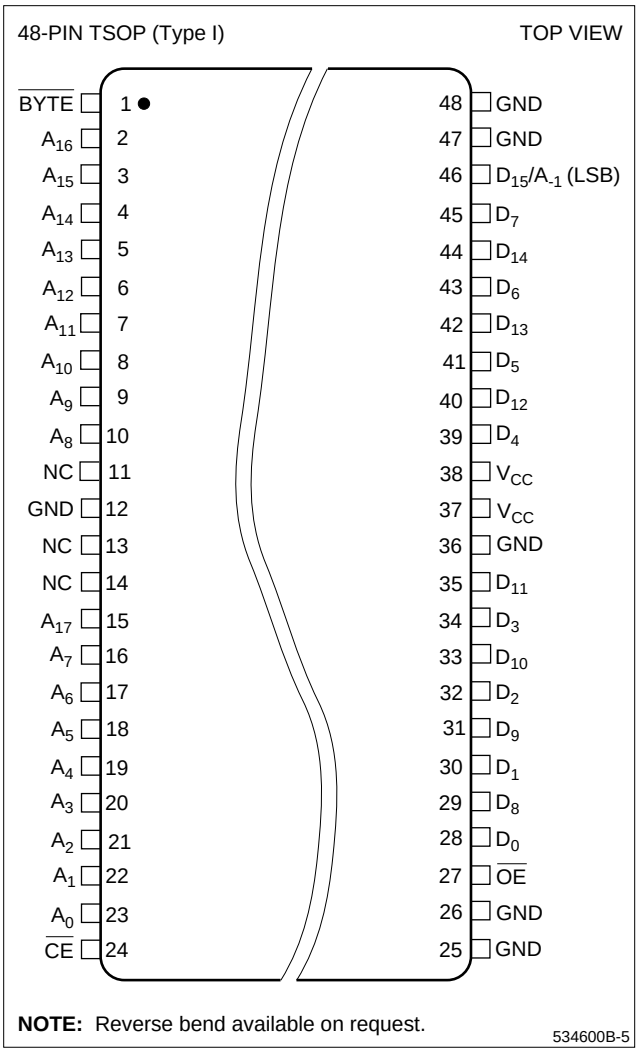
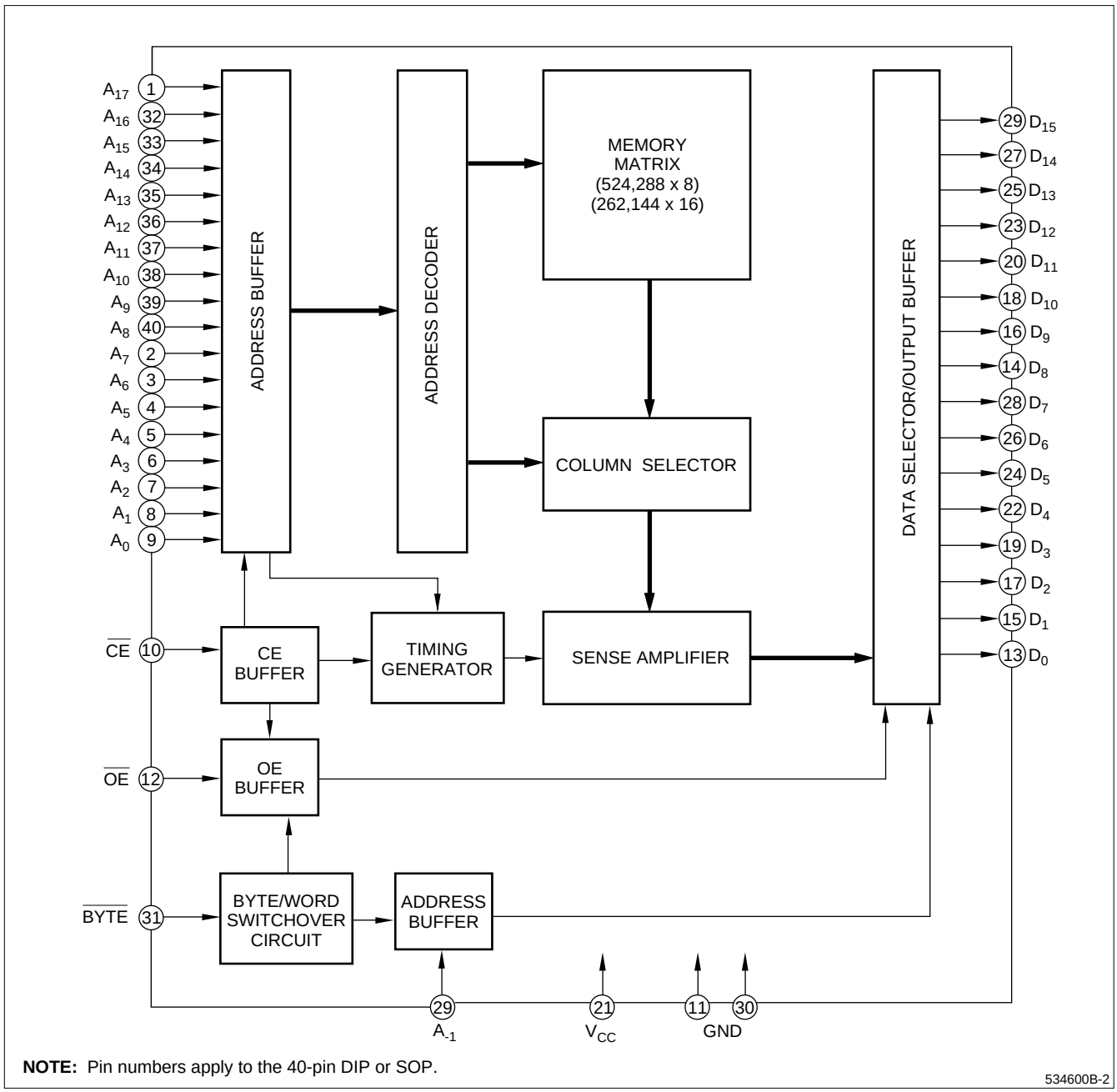


Figure 2. Pin Connections for TSOP Package



NOTE: Pin numbers apply to the 40-pin DIP or SOP.

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Figure 3. LH534600B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE MODE)	1
$A_0 – A_{17}$	Address input	
$D_0 – D_{15}$	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1

SIGNAL	PIN NAME	NOTE
$\overline{CE}$	Chip enable input	
$\overline{OE}$	Output enable input	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 – D_7	D_8 – D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Not selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Not selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 – D_7	D_8 – D_{15}	Operating (I_{CC})	
L	L	L	L	Byte	D_0 – D_7	High-Z	Operating (I_{CC})	
L	L	L	H	Byte	D_8 – D_{15}	High-Z	Operating (I_{CC})	

NOTE:
1. The input state of $\overline{BYTE}$ pin must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		–0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns			75	mA	2
	I_{CC2}	t_{RC} = 1 µs			65		
	I_{CC3}	t_{RC} = 100 ns			70	mA	3
	I_{CC4}	t_{RC} = 1 µs			60		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			55	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			50	ns	1
OE to ouput in High-Z	t_{OHZ}			50	ns	

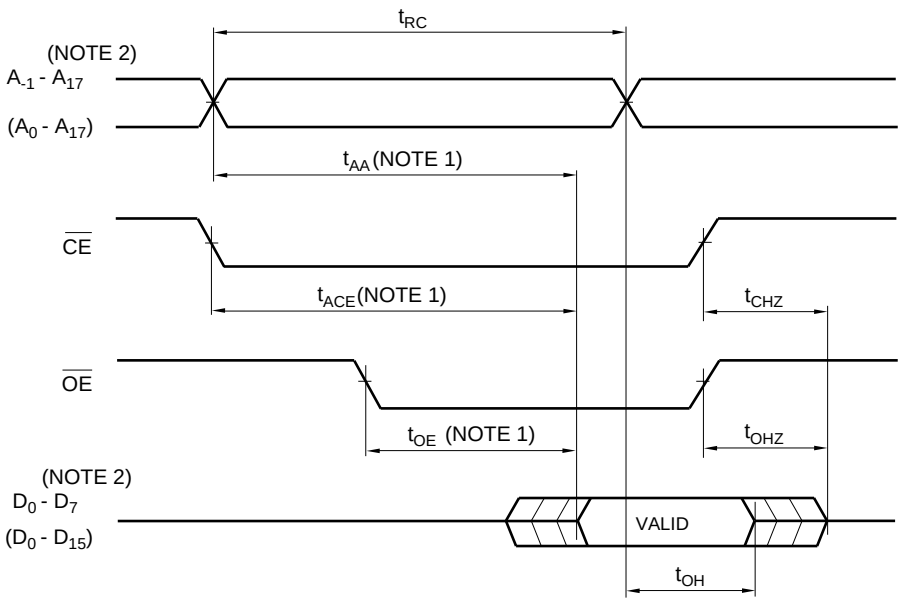
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input and output enable input, respectively have been met.
2. Apply to byte mode. Signals in parentheses apply to word mode.

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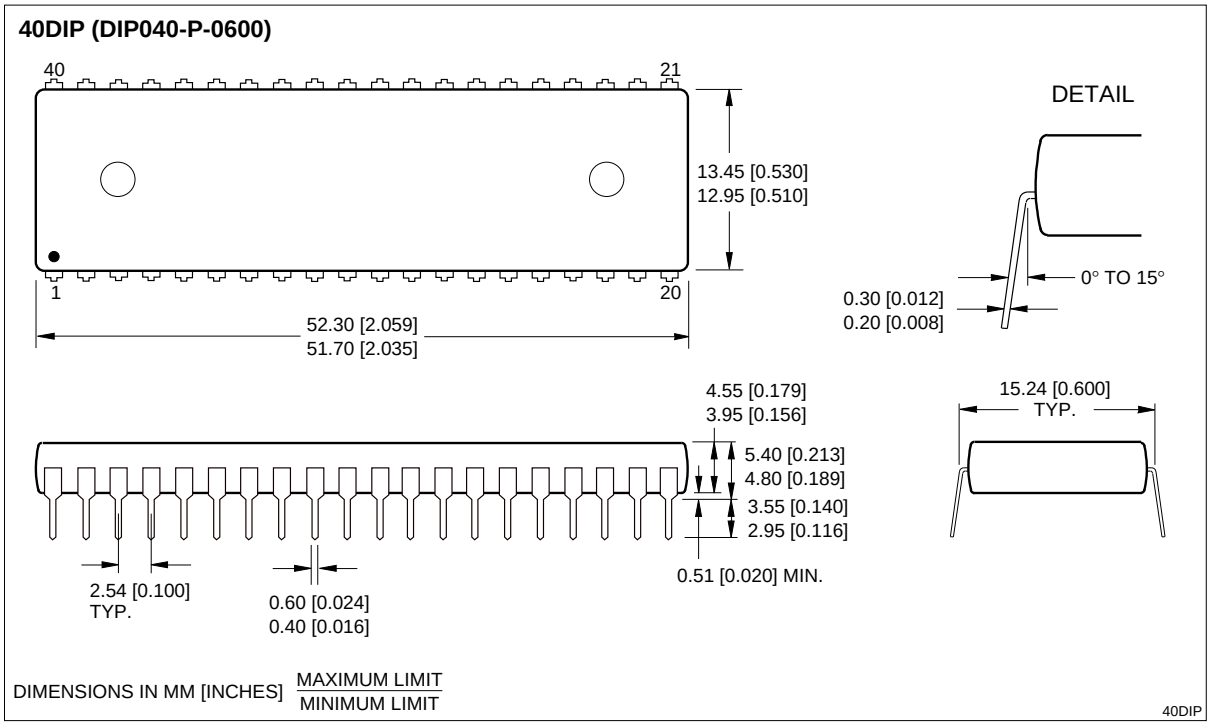
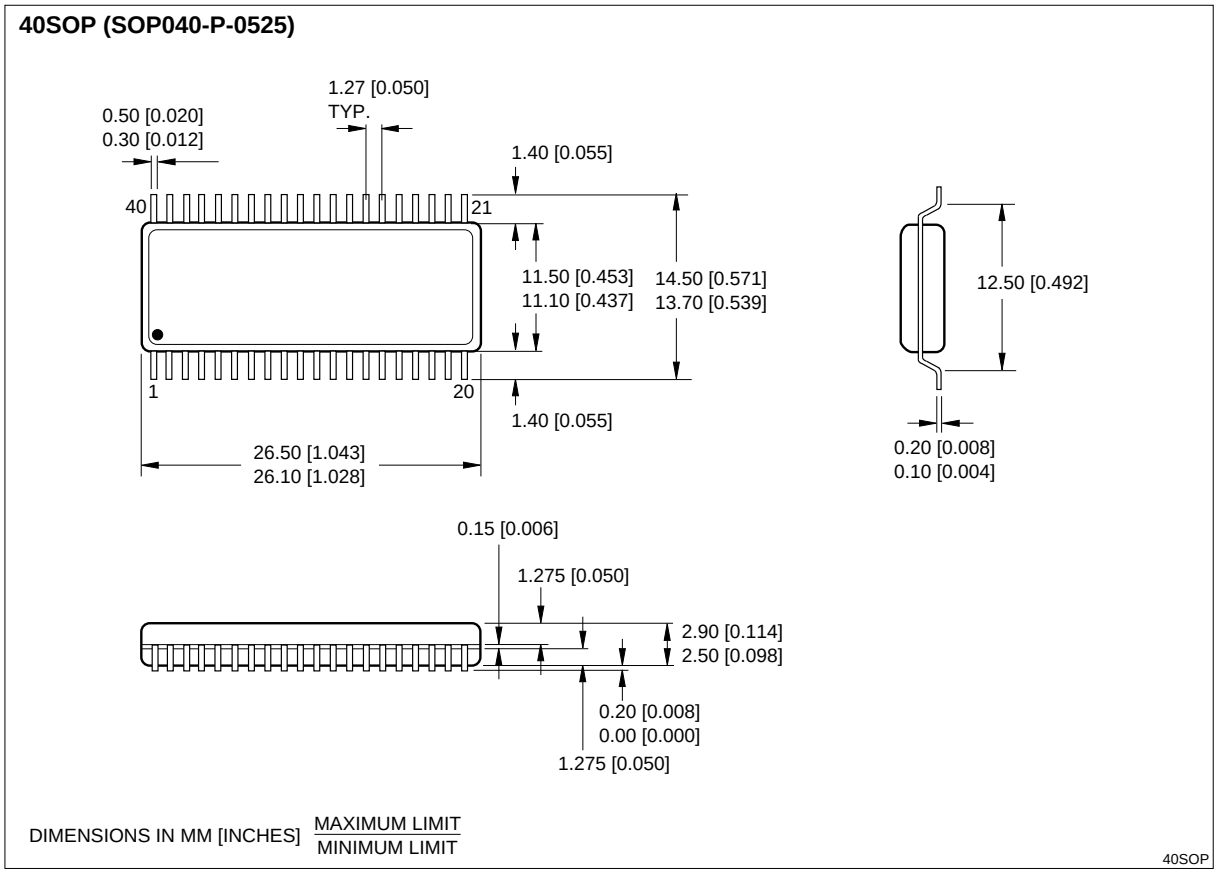
Figure 4. Timing Diagram

PACKAGE DIAGRAMS

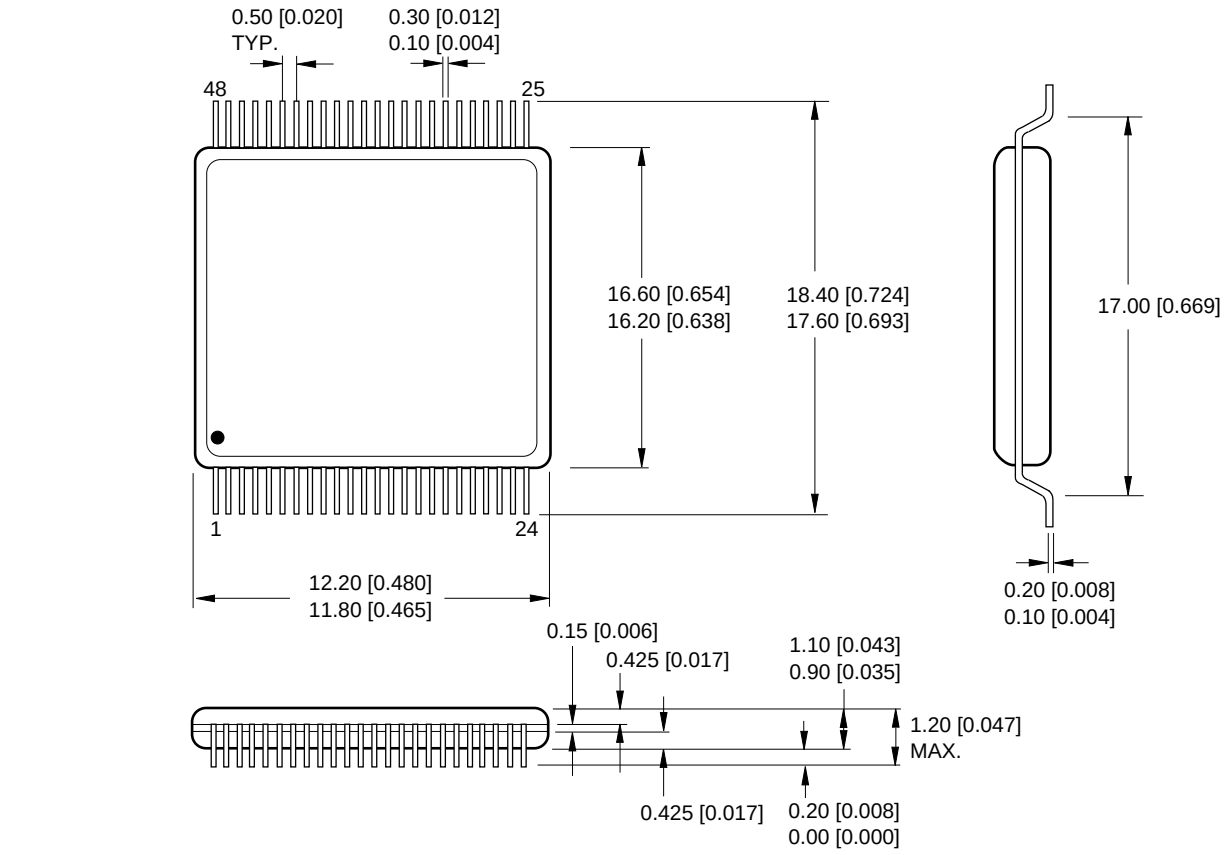


40-pin, 600-mil DIP



40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH534600B — Device Type

X — Package

- D 40-pin, 600-mil DIP (DIP040-P-0600)
- N 40-pin, 525-mil SOP (SOP040-P-0525)
- T 48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 4M (512K x 8 or 256K x 16) Mask Programmable ROM

Example: LH534600BD (CMOS 4M (512K x 8 or 256K x 16) Mask Programmable ROM, 40-pin, 600-mil DIP)

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